DESIGN SPACE EXPLORATION OF NETWORK-ON-CHIP: A SYSTEM LEVEL APPROACH

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The growing complexity of system-on-chip is requiring communication resources that can only be provided by a highly scalable communication infrastructure. This is simplified by Network on Chip (NoC) architectures. The problem of topological mapping of intellectual properties (IPs) on the tile of a mesh-based NoC to minimize energy and maximum bandwidth requirement is a NP-hard problem. So, in this paper, we address the problem of topological mapping of intellectual properties (IPs) on the tile of a mesh-based NoC to minimize energy and maximum bandwidth requirements using multi-objective genetic algorithm. We have also considered "many-many" mapping between switch and cores(tiles) instead of "one-one" mapping. The evaluation performed on three randomly generated benchmarks and a real application (an M-JPEG encoder) to conform to the efficiency, accuracy and scalability of the proposed approach.

Categories and Subject Descriptors: B.7 [**Integrated Circuit**]: System Level Synthesis I.2 [**Artificial Intelligence**]: Multi-objective genetic algorithm
General Terms: Design and Modeling
Additional Key Words and Phrases: NoC optimization, Energy, Performance

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1. INTRODUCTION

Network on Chip (NoC) has been proposed as a solution for the communication challenges like propagation delays, scalability, infeasibility of synchronous communication etc. in a nano scale regime [5-6]. To meet these challenges under the strong time-to-market pressure, it is essential to increase the reusability of components and system architectures in a plug and play fashion (J. Hu and R. Marculescu. 2003). Simultaneously, the volume of data and control traffic among the cores grows. So, it is essential to address the communication-architecture synthesis problem through mapping of cores onto the communication architecture (K. Lahiri, A. Raghunathan, and S. Dey, 2000). Therefore this paper focuses on communication architecture synthesis to minimize the energy consumption and communication delay by minimizing maximum link bandwidth using many-many mapping between resources and switches.

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The proposed communication synthesis task has been solved in two phases as shown in Figure1. The first phase (P-1) is called computational synthesis. The input to P-I is a task graph. The task graph consists of tasks as vertices and direct edges represent volume of data flowing between two vertices and their data dependencies. The output of P-I is a core communication graph (CCG) characterized by a library of interconnection network elements and performance constraints. The core communication graph consists of processing and memory elements are shown by P/M in the Figure1. The directed edges between two blocks represent the communication trace. The communication trace is characterized by bandwidth (b_{sd}) and volume (v_{sd}) of data flowing between different cores. The second phase (P-II) is basically called a communication synthesis. The input to the P-II communication synthesis problem is the CCG. The output of the P-II is the energy and throughput synthesizes NoC back bone architecture shown in Figure1.

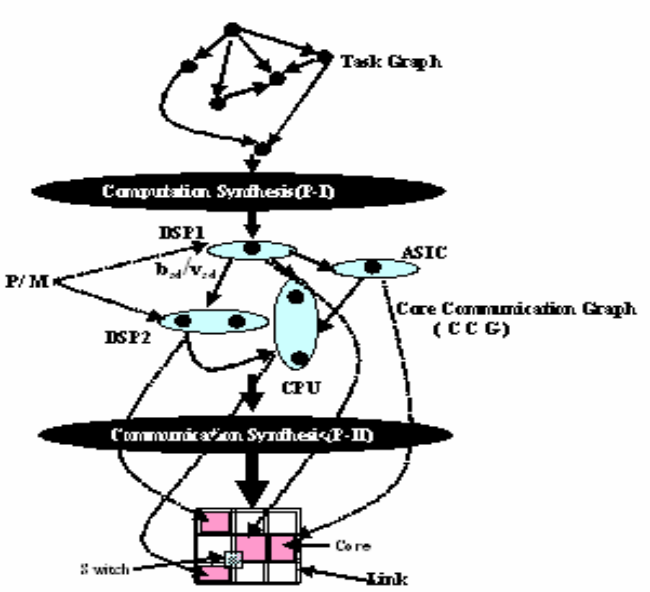

Figure 1: Mappings for NoC synthesis problems

In this paper we address the problem of mapping the core onto NoC architecture to minimize energy consumption and maximum link bandwidth. Both of the above stated objectives are inversely proportional to each other. The above stated problem is an NP-hard problem (M. R. Garey and D. S. Johnson 1979). So, genetic algorithm is a suitable candidate for solving the multi-objective problem (Luca Benini and Giovanni De Micheli 2002). The optimal solution obtained by our approach saves more than 15% of energy on average in comparison to other existing approaches. Experimental result shows that our proposed model is superior in terms of quality of result and execution time in compare to other approaches.

The paper is organized as follows. We review the related work in Section 2. Section 3 and Section 4 describes the problem definition and the energy model assumed in this paper. Section 5 represents the multi-objective genetic algorithm formulation for the problem. Section 6 discusses the basic idea and problem formulation for the proposed approach. Experimental results are discussed in Section 7. Finally, a conclusion is given in Section 8.

2. RELATED WORK

The problem of synthesis in mesh-based NoC architectures has been addressed by different authors. Hu and Marculescu (J. Hu and R. Marculescu. 2003) present a branch and bound algorithm for mapping IPs/cores on a mesh-based NoC architecture that minimizes the total amount of power consumed in communications. De Micheli (S. Murali and G. D. Micheli 2004) address the problem under the bandwidth constraint with the aim of minimizing communication delay by exploiting the possibility of splitting traffic among various paths. Lei and Kumar (T. Lei and S. Kumar 2003) present an approach that uses genetic algorithms to map an application on a mesh-based NoC architecture. The algorithm finds a mapping of the vertices of the task graph on the available cores so as to minimize the execution time. However these papers do not solve certain important issues. The first relates to the evaluation model used. In most of the approaches the exploration model decides the mapping to explore the design

space without taking important dynamic effects of the system into consideration. Again in the above mentioned works, in fact, the application to be mapped is described using task graphs, as in (T. Lei and S. Kumar 2003), or simple variations such as the core graph in (S. Murali and G. D. Micheli 2004) or the application characterization graph (APCG) in (J. Hu and R. Marculescu. 2003). These formalisms do not, however, capture important dynamics of communication traffic. The second problem relates to the optimization method used. It refers in all cases to a single performance index (power in (J. Hu and R. Marculescu. 2003), performance in (S. Murali and G. D. Micheli 2004; T. Lei and S. Kumar 2003). So the optimization of one performance index may lead to unacceptable values for another performance index (e.g. high performance levels but unacceptable power consumption). Recently, Jena and Sharma (Jena, R.K, Sharma, G.K. 2006) proposed a model that consider "many-many" mapping between core and tiles using multi-objective genetic algorithm. But they used core communication graph as the input to their model. We therefore think that the problem of mapping can be more useful to solved in a multi-objective environment starting from the higher level of input as compared to the model discussed in (Jena, R.K, Sharma, G.K. 2006). The contribution we intend to make in this paper is to propose a multi-objective approach to solving the synthesis problem on a mesh-based NoC architecture, where we take the task graph as input. The approach, we will use is evolutionary computing techniques based on genetic algorithm to explore the mapping space with the goal to optimize maximum link bandwidth and energy consumption (both computational and communication).

3. PROBLEM DEFINITION

3.1. Task Graph (TG)

A Task Graph (TG) is a digraph, G (V, E), where each vertex v Є V represents a task and each edge e Є E is a weighted edge, where weight signifies the volume of data flowing through the edge. Every edge also represents the data dependency between the connecting vertices.

3.2. Core Communication Graph (CCG)

A Core Communication Graph (CCG) is a digraph, G(V,E), where each vertex v Є V represents a core and e Є E is a communication edge having two attributes, denoted by b_{sd} and v_{sd} . The b_{sd} and v_{sd} are the required bandwidth and total volume of communication for each edges respectively.

3.3 Communication Structure

The 2-D mesh communication architecture has been considered for its several desire properties like regularity, concurrent data transmission and controlled electrical parameters (J. Hu and R. Marculescu. 2003;S. Kumar et al. 2002). Figure 2 shows how a tile (T) is binding with its surrounding switches(S) in a 2-D mesh NoC architecture. Each tile is a square surrounded by '4' switches and links. A resource in a tile can be connected to maximum '4' switches as shown in the Figure 2. Each switch is connected to its neighboring switches via two unidirectional links. To prevent the packet loss due to the multiple packets approaching to the same output port, each switch has small buffers (registers) to temporarily store the packets. Each resource has 4 Resource Network Interfaces (RNIs) to connect to the network via switches. RNIs are responsible for packetizing and depacketizing the communication data. We implement static XY wormhole routing in this paper because:

i) it is easy to implement in a switch.
ii) it doesn't require packet ordering buffer at the destination.
iii) it is free of deadlock and live lock (N. Banerjee, P. Vellanki, and K. S. Chatha 2004; S. Murali and G. D. Micheli 2004).

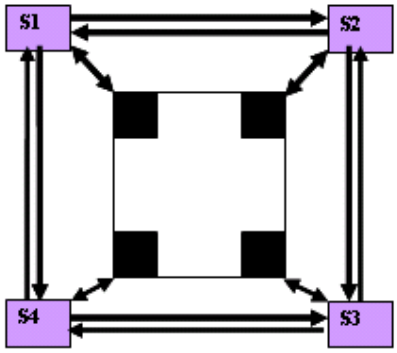

Figure 2: Communication Structure

4. ENERGY MODEL

Energy minimization is one of the major challenging tasks in NoC design. In (T. T. Ye, L. Benini, and G. D. Micheli 2002), Ye et al. first define the bit energy metric of a router as the energy consumed when a single bit of data goes through the router. In (J. Hu and R. Marculescu. 2003), Hu et al. modify the bit energy model so that it is suitable for 2D mesh NoC architecture. They derives mathematical expression for bit energy consume, when the data transfer from switch i to switch j is given by

$$E_{i,j\,bit} = (h_{ij} + 1)\, E_{Sbit} + h_{ij}\, E_{Lbit} \quad \text{---------- (1)}$$

E_{Sbit} and E_{Lbit} are the energy consumed in the switches and links respectively. The variable h_{ij} represent the number of links on the shortest path. As per the expression, the energy consumptions depends on the hop distance (h_{ij}) between switch i and j because E_{Sbit} and E_{Lbit} are constants. Note E_{Sbit} is the energy consumption due to switches, depending on the number of ports in the switches. But in our case the total energy is the sum of communication and computation energies, i.e

$$E_{i,j\,bit} = (h_{ij} + 1)\, E_{Sbit} + h_{ij}\, E_{Lbit} + E_{Com} \quad \text{----------(2)}$$

E_{Comp} is the computational energy consumption.

The following sections discuss the basic ideas of problem formulation using multi-objective optimization paradigm.

5. MULTI-OBJECTIVE OPTIMIZATION

Definition:
A general multi-objective optimization problem is defined as:
Minimize $f(x) = (f_1(x), \ldots, f_k(x))$ subject to $x \in X$, where x represents a solution and X is a set of feasible solutions.
The objective function vector f (x) maps a solution vector x in decision space to a point in objective space.

In general, in a multi-objective optimization problem, it is not possible to find a single solution that minimizes all objectives simultaneously. Therefore, one is interested to explore a set of solutions, called the pareto optimal set, which is not dominated by any other solution in the feasible set. The corresponding objective vectors of these Pareto optimal points, named efficient points, form the Pareto front on the objective space.

Definition:
We say , a solution (x)dominates another solution (x*) iff $i \in \{1,\ldots,k\}$
$f_i(x) \leq f_i(x^*)$ and there exists at least one $i \in \{1,\ldots, k\}$ such that $f_i(x) < f_i(x^*)$.

The most traditional approach to solving a multi-objective optimization problem is to aggregate the objectives into a single objective by using a weighting mean. However this approach has major drawbacks. It is not possible to locate the non-convex parts of the pareto front and it requires several consecutive runs of the optimization program with different weights. Recently, there has been an increasing interest in evolutionary multi-objective optimization. This is because of the fact that

evolutionary algorithms (EAs) seem well-suited for this type of problems (C. A. Coello,2002), as they deal simultaneously with a set of possible solutions called population. This allows us to find several members of the pareto optimal set in a single run of the algorithm. To solve the synthesis problem as discussed in Section 4, we used the multi-objective genetic algorithm.

5.1 A Multi-Objective Genetic Algorithm

In order to deal with the multi-objective nature of NoC problem we have developed genetic algorithms at different phases in our model. The algorithm starts with a set of randomly generated solutions (population). The population size remains constant throughout the GA. Each iteration, the solutions are selected according to their fitness quality (ranking) to form new solutions (offspring). Offspring are generated through a reproduction process (Crossover, Mutation). In a multi-objective optimization, we are looking for all the solutions of best compromise. The best solutions encountered over generations are mapped (stored) into a secondary population called the "Pareto Archive". In the selection process, solutions can be selected from this "Pareto Archive"(elitism). A part of the offspring solutions replace their parents according to the replacement strategy. In our study, we used elitist non-dominated sorting genetic algorithm NSGA-II by Deb et al. (Deb K,2002).

6. PROBLEM FORMULATION

6.1 Basic Idea

Like other algorithms in the area of design automation, the algorithm of NoC communication architecture is a hard problem. Our attempt is to develop an algorithm that can give near optimal solution within reasonable time. Genetic algorithms have shown the potential to achieve the dual goal quite well (Jena, R.K, Sharma, G.K. 2006; K. Srinivasan and Karam S. Chatha 2005; T. Lei and S. Kumar 2003; A. D. Pimentel et al, 2002).

As shown in Figure 3 and discussed in Section 1, the problem is solved in two phases. The first phase (P-I) is basically a task assignment problem (TA-GA). The input to the problem is a TG. We assume that all the edge delays are a constant and equal to Average Edge Delay (AED) (N. Banerjee, P. Vellanki, and K. S. Chatha 2004). The output of the first phase is a Core Communication Graph (CCG). The task of the second phase is Core-Tile-switch Mapping using genetic algorithm (CTS-GA). The next section discusses each of the phases in detail.

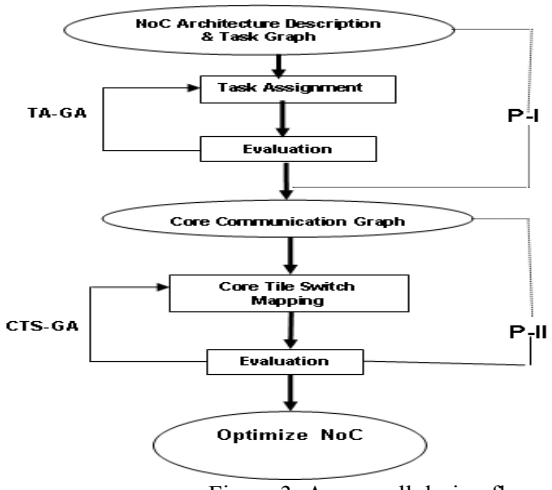

Figure 3: An overall design flow

6.1.1 Task Assignment Problem (TA-GA)

Given a task graph (TG) (with all edge delay are constant and equal to average edge delay) and IPs with specifications matrix containing cost and computational energy. The main objectives of this phase are to assign the tasks from the task graph to the available IPs in order to: (i) minimize the computational energy by reducing the power consumption. (ii) Minimize the total cost of the resources. The above said problem is a NP-hard multi-objective problem. We propose a multi-objective genetic algorithm based on principle of NSGA-II. Generally, in genetic algorithm, the chromosome is the representation of solution to the problem. In this case the length of each chromosome is proportional to the number of nodes in a task graph. The i-th gene in the chromosome identifies the IP which is assigns the i-th node in the task graph. One example of chromosome encoding is given in Figure 5. Each gene

(node in TG) in the chromosome contains an integer which represents an IP. Every IP is chosen from the list of permissible IPs for that task. As shown in the Figure 4 the task number 2 in the task graph is assigned to IP number 7 which is chosen from set of IPs {7, 8, and 17}. We consider a single point crossover to generate the offspring's. As for mutation operation, we consider the mutation by substitution i.e. at a time a gene in a chromosome is chosen with some random probability and the value in the gene is substituted by one of the best permissible values (i.e the index value of a IP) for the gene. The aim is to assign more tasks to a particular IP to reduce the communication between IPs i.e to minimize the number of IPs used for a task graph.

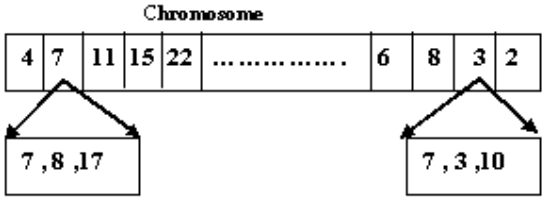

Figure 4: Chromosome encoding for task assignment.

6.1.2 Core-Tile-Switch Mapping (CTS-GA)

After the optimal assignment of tasks to the IPs, we get a Core Communication Graph (CCG) as shown in the Figure4. The input to this mapping task CT-GA is a CCG and a structure of NoC back bone. In our case it is an n×m mesh. The objectives of the mapping are (i) to reduce the average communication distance between the cores (i.e to reduce number of switches in the communication path). (ii) to maximize throughput(i.e minimize the maximum link bandwidth) under the communication constraint.

Core-tile mapping is a multi-objective mapping. So we use genetic algorithm based on NSGA-II. Here the chromosome is the representation of the solution to the problem, which in this case is described by the mapping. Each tile in the mesh has an associated gene which identified the core mapped to the tile. In n×m mesh, for example the chromosome is formed by n×m genes. The i-th gene identifies the core in the tiles (row ($\lceil (i / n) \rceil$) and column (i % n)). The crossover and mutation operators for this mapping have been defined suitably as follows:

Crossover:
The crossover between two chromosomes C_1 and C_2 is generated a new chromosome C_3 as follows. The optimal (dominated) mapping between C_1 and C_2 is chosen. Its hot core (the hot core is the IP required maximum communication) is remapped to a random tile in the mesh, resulting a new chromosome C_3.

Algorithm Crossover ($\mathbf{C_1}$, $\mathbf{C_2}$)
{
If ($\mathbf{C_1}$ *dominate* $\mathbf{C_2}$)
$\mathbf{C_3} = \mathbf{C_1}$;
e l s e
$\mathbf{C_3} = \mathbf{C_2}$;
Swap ($\mathbf{C_3}$, Hot ($\mathbf{C_3}$), random({1,2,3,…….m×n}));
Return ($\mathbf{C_3}$);
}
The function Swap(C, i, j) exchanges the i-th gene with j-th gene in the chromosome C.

Mutation:
The mutation operator act on a single chromosome (C) to obtain a muted chromosome C^0 as follows. A tile T_s from chromosome C is chosen at random. Indicating the core in the tile T_s as c_s and c_t as the core with which c_s communicates most frequently, c_s is remapped on a tile adjacent to T_s so as to reduce the distance between c_s and c_t,, thus obtaining the mutated chromosome C^0. The algorithm, given below describes the mutation operator. The RandomTile(C) function gives a tile chosen at random from chromosome C. The MaxCommunication(c), finds the core with which *c* communicates most frequently. The Row(C, *T*) and Col(C, *T*) functions give the row and column of the tile *T* in chromosome C respectively. Finally, the Uper, Lower, Left, Right(C, *T*) functions find the tile to the north, south, east and west of the tile *T* in chromosome C.

Algorithm Mutate (C)
{
Chromosome $\mathbf{C}^0 = \mathbf{C}$;
Tile T_s = Random Tile ($\mathbf{C}^0$);
Core $c_s = \mathbf{C}^{0\text{-}1}(T_s)$;
Core c_t = MaxCommunication (c_s);
Tile $T_t = \mathbf{C}^0$ (c_t);
if (Row($\mathbf{C}^0$, T_s) < Row($\mathbf{C}$, T_t))
T^0_s = Upper ($\mathbf{C}^0$, T_s) ;
else if (Row($\mathbf{C}^0$, T_s) > Row($\mathbf{C}^0$, T_t))
T^0_s = Lower($\mathbf{C}^0$, T_s) ;
else if (Col($\mathbf{C}^0$, T_s) < Col($\mathbf{C}^0$, T_t))
T^0_s = Left($\mathbf{C}^0$, T_s) ;
else
T^0_s = Right($\mathbf{C}^0$, T_s) ;
Swap ($\mathbf{C}^0$, T_s , T^0_s) ;
Return **(** $\mathbf{C}^0$);
}

7. EXPERIMENTAL RESULTS

This section presents the results of our multi-objective genetic formulation (MGA). The final results i.e the result obtained after completion of CTS-GA are compared with PBB algorithm (J. Hu and R. Marculescu. 2003) and MGAP algorithm (Jena, R.K, Sharma, G.K. 2006). For TA-GA, we consider NSGA-II multi-objective evolutionary algorithm technique with crossover probability 0.98 and mutation probability 0.01. For CT-GA, we consider NSGA-II with our introduced new crossover and mutation operator. Table 1 shows the bit-energy value of a link and a switch (**4×4)** assuming 0.18 μm technology.

$\mathbf{E_{Lbit}}$	$\mathbf{E_{Sbit}}$
5.445pJ	0.43pJ

Table 1: Bit energy values for switch and link

The value of $\mathbf{E_{Lbit}}$ is calculated from the following parameters.
(1) length of link (2mm) (2) capacitance of wire (0.5fF/ μm) (3)voltage swing (3.3V)
In our experiment, we consider three random applications, each consisting of 9, 14 and 18 cores respectively. After P-I, we found that the CCG of all three benchmarks consists of up less than 9 cores, which can be mapped on to a 3×3 mesh NoC architecture. It has been seen that the required bandwidth of an edge connected two different nodes is uniformly distributed over the range [0, 150Mbytes].The traffic volume of an edge also has been uniformly distributed over the range [0, 1Gbits]. Figure-5 shows the maximum link bandwidth utilization of three benchmarks. It is clear from the figure that our approach (MGA) saves more than 5% link bandwidth as compare to MGAP and around 15% in comparison to PBB. Figure-6 shows that our approach saves more than 70% of energy consumptions in compare to PBB(on average) and around 10% in comparision to MGAP.

The real time application is a modified Motion-JPEG (M-JPEG) encoder. Which differs from traditional encoders in three ways: (i) it only supports lossy encoding while traditional encoders support both lossless and lossy encodings (ii) it can operate on YUV and RGB video data whereas traditional encoders usually operate on the YUV format, and (iii) it can change quantization and Huffman tables dynamically while the traditional encoders have no such behavior. We omit giving further details on the M-JPEG encoder as they are not crucial for the experiments performed here. Interested readers may refer to the paper by A. D. Pimentel et. al.

Figure 7 shows the bandwidth requirements and energy consumptions for M-JPEG encoder application. From the figure it is clear that our approach out performs other approaches. Figure 8 shows the behavior of NSGA-II with respect to number of generations.

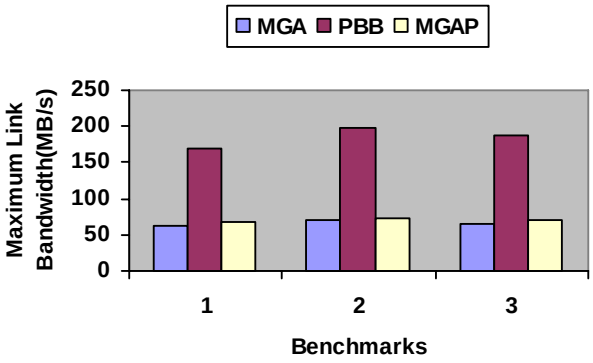

Figure 5: Maximum Link Bandwidth comparisons for three random benchmarks

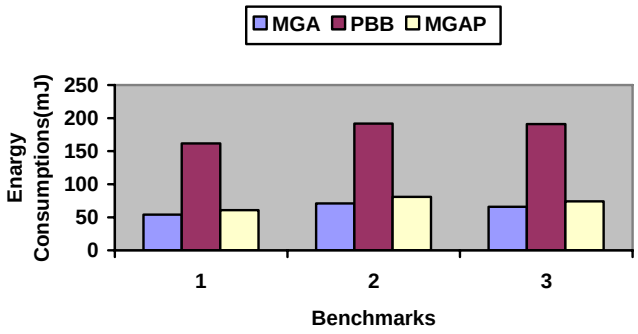

Figure 6: Energy comparisons for three random benchmarks

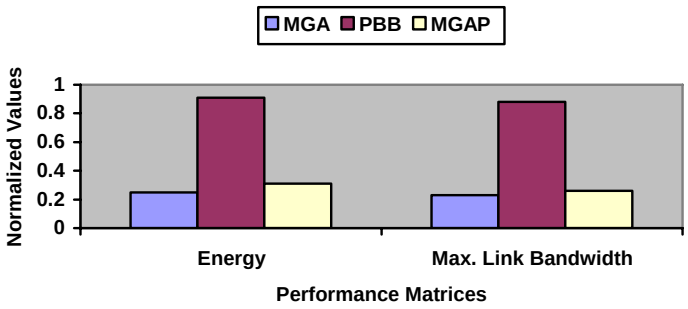

Figure 7: Maximum Link Bandwidth and Energy comparisons for M-JPEG

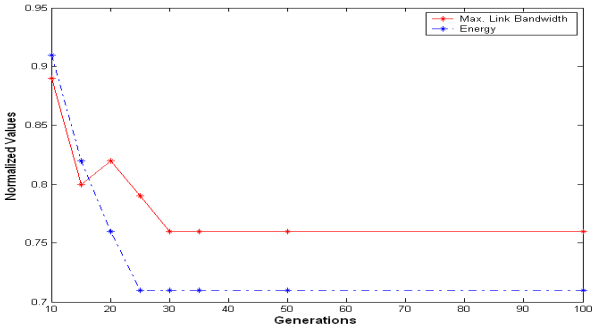

Figure 8 : M-JPEG Encoder performance using NSGA-II

8. CONCLUSION

In this paper we have proposed a model for topological mapping of IPs/cores in a mesh-based NoC architecture with many to many mappings between cores to switches. The approach uses heuristics based on multi-objective genetic algorithms (NSGA-II) to explore the mapping space and find the pareto mappings that optimize maximum link bandwidth and performance and power consumption. The experiments carried out with three randomly generated benchmarks and a real application (M-JPEG encoder system) confirms the efficiency, accuracy and scalability of the proposed approach. Future developments will mainly address the definition of more efficient genetic operators to improve the precision and convergence speed of the algorithm. Evaluation will also be made of the possibility of optimizing mappings by acting on other architectural parameters such as routing strategies, switch buffer sizes, etc.

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