Characterizing the Maximum Queuing Delay of a Packet Switch

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ABSTRACT
The queuing delay which is suffered by a packet that is transiting a packet switch has the most adverse effect on the delay performance of the switch. Being able to estimate the maximum queuing delay which any packet may suffer in a packet switch will make it possible to design upper bounded end-to-end delay switched networks, which are very important in today's delay sensitive networks. In this paper, we have characterized the maximum queuing delay of a packet switch; a characterization, which is in consonance with the definition of maximum queuing delay in literature.

KEYWORDS: Maximum Queuing Delay, Packet switch, End-To-End Delay

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1. INTRODUCTION
Queuing delay is the time between when a packet is assigned to a queue for transmission and when it starts being transmitted; during this time, the packet waits while other packets in the queue are transmitted. (Bertsekas and Gallager, 1992, p.150) The queuing delay has the most adverse effect on packet delay in a switched network. According to Song (2001), any frame traveling through the switches in its path from origin node to destination node without experiencing any buffering (queuing) has the minimum end-to-end delay. Queuing delay builds up at the output port of a switch because the port may receive packet from several input ports, that is, packets from several input ports that arrive simultaneously may be destined for the same output port. (Anurag, Manjunath and Kuri, p.121) If input and output links are of equal speed, and if only one input link feeds an output link, then a packet arriving at the input will never find another packet in service and hence, will not experience queuing delay. Message buffering occurs whenever the output port cannot forward all input messages at a time and this corresponds to burst traffic arrival; the analysis of buffering delay therefore, depends on knowledge of the input traffic patterns. (Song, 2001; Song et al., 2002) Because of the adverse effect which the queuing delay of a packet switch can have on the delay performance of the switch, there is the need to characterize the maximum queuing delay which a packet may suffer in a packet switch. This will make the designs of upper bounded end-to-end delay switched networks possible. In the work of Georges, Divoux, and Rondeau (2005), an expression for the maximum

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queuing delay of a packet switch was obtained; but the expression is not a reflection of the definition of a packet switch's maximum queuing delay in literature. Taking a cue from this work, we have characterized the maximum queuing delay of a packet switch; a characterization, which is in consonance with the definitions of queuing (maximum queuing) delay in literature.

2. DERIVATION OF AN EXPRESSION FOR THE MAXIMUM QUEUING DELAY OF A PACKET SWITCH

The output port of a packet switch can be modeled as a FIFO (first-in-first-out) queue. The FIFO queue can be viewed as a degenerate form of FCFS (first-come-first-served) multiplexer (the multiplexer on the other hand, has two or more input links and a single output link; its function is to merge the streams arriving on the input links onto the output link). (Cruz, 1991) The FIFO queue has one input link and one output link. The input link has transmission capacity C_{in} and the output link has transmission capacity C_{out}. The FIFO is defined simply as follows. Data that arrives on the input link is transmitted on the output link in FCFS order as soon as possible at the transmission rate C_{out}. (Georges, Divoux, and Rondeau, 2005; Cruz, 1991) For example, if a packet begins to arrive at time t_0 and if no backlog exists inside the FIFO at time t_0, then the packet also commences transmission on the output link at time t_0. It is assumed that $C_{in} \geq C_{out}$ so that this is possible; if C_{in} were less than C_{out}, then this would be impossible to do, as the FIFO would 'run out' of data to transmit immediately following time t_0, before the packet could be transmitted at rate $C_{out.}$ (Cruz, 1991)

Suppose that the rate of the input stream to the FIFO queue is given as $R_{in}(t)$; if the size of the backlog inside the FIFO at time t is given by $W_{Cout}(R_{in})(t)$, the j^{th} packet which arrives at time S_j must wait for all the current backlog, and this backlog gets transmitted at rate C_{out}. It follows that the j^{th} packet commences exit from the FIFO queue at time $t_j = S_j + d_j$, where d_j is given by Eq. (1).

$$d_j = \frac{1}{C_{out}} W_{Cout}(R_0)(S_j). \quad (1)$$

and $t_j = S_j + d_j$

S_j = time at which the j^{th} packet starts arriving at the FIFO queue
d_j = time spent by the j^{th} packet in the FIFO queue before being transmitted at rate C_{out}
= maximum delay of the j^{th} packet in the FIFO queue
t_j = time at which the j^{th} packet commences exit from the FIFO queue

The FIFO queue is illustrated in Figure 1.

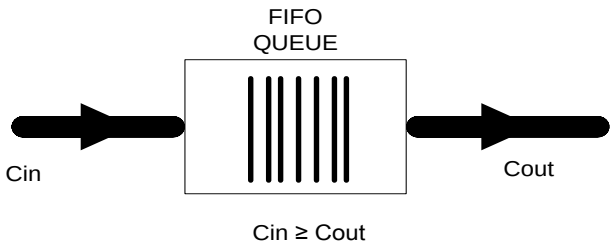

Fig. 1. Illustration of a FIFO queue

If R ~ (σ, ρ), where R = the rate function of a traffic stream,
ρ > 0 is an upper bound on the long-term average rate of the traffic flow,
σ ≥ 0 is the burstiness constraint of the traffic stream (the maximum amount of data that can arrive in a burst), then the function $W_\rho(R)$ was defined for all times by Cruz (1991) as follows:

$$W_\rho(R)(t) = \max_{s \leq t} \left[\int_s^t R - \rho(t-s) \right]. \quad (2)$$

Where $W_\rho(R)(t)$ = size of the backlog in a system (that is, the amount of unfinished work) at time t in a work-conserving system which accepts data at a rate described by the rate function R, and transmits data at the rate ρ while there is work to be done(data to be transmitted).

The presentation in this paper of course implies the assumption of output buffering, which is what is implemented in switches, as it eliminates head-of-line (HOL) blocking
(Georges, Divoux, and Rondeau, 2005; Song, 2001), and since buffering delays occur in switches during burst traffic arrival periods when the output port cannot forward all arrived packets in a particular time period in the same time period (Sven, Ales, and Stanislav, 2008; Ryousei et al., 2006; Song, 2001), it may therefore, be necessary to have a knowledge of the input traffic pattern. (Song et al., 2002; Song, 2001)

An arriving packet to a FIFO queue has to wait for the backlog in the queue to be zero before it will be forwarded on the output link at rate C_{out}, where, C_{out} = bit rate of the output link (switch port).
From Eq. (2), the backlog inside the queue at time t is given as:

$$Wc_{out}(R)(t) = \max_{s \le t}\left[\int_s^t R_{in}(t)dt - C_{out}(t-s)\right] \quad (3)$$

Where, $R_{in}(t)$ = rate function of the incoming traffic stream at time t.

Putting Eq. (3) into Eq. (1), we have:

$$d_j = \frac{1}{C_{out}} \times \max_{s \le s_j}\left[\int_s^{s_j} R_{in}(t)dt - C_{out}(s_j - s)\right] \quad (4)$$

Since our intention is to provide a maximum bound on this delay (d_j), the challenge here is, how do we determine the interval [s, s_j] for which d_j is maximum? This will have to correspond to the maximum burst traffic arrival period of the incoming traffic. But C_{out} is fixed, this is because, the FIFO queue is a degenerate FCFS MUX (Cruz, 1991), and we assume that the FCFS MUX is work-conserving; that is, if B(t) is the backlog at time t, and B(t)>0 at any instant of time t, then, $R_{out}(t) = C_{out}$ (Cruz, 1991). So definitely, the interval [s, s_j] where dj is maximum only depend on the arrival process of the traffic $R_{in}(t)$.

To determine a possible traffic arrival interval where, d_j would be, maximum, recall that, R_{in} is the rate function of the incoming traffic stream;

$\forall s_j \ge s$, $\int_S^{Sj} R_{in}(t)\,dt$ is the amount of traffic that has arrived in the closed interval [s, s_j].

Given $\sigma \ge 0$, and $\rho \ge 0$, we write $R_{in} \sim (\sigma, \rho)$, if and only if for all s, s_j satisfying $s_j \ge s$, there holds:

$$\int_S^{Sj} Rin(t)dt \le \sigma + \rho(s_j - s) \quad (5)$$

Where σ = the maximum amount of traffic that can arrive in a burst, and,
ρ = the long term average rate of traffic arrivals

Similarly, if b is any function defined in the non-negative reals, and $R_{in} \sim b$, we can write (Georges, Divoux, and Rondeau, 2005; Cruz, 1991):

$$b(t) = \sigma + \rho t \quad (6)$$

Where b(t) is an affine arrival curve.

In consonance with the description of the physical layer switch system in (US Patent No. 5889776, 2008), that the switching circuit of a switch establishes a link between two ports specified by the source address and the destination address that is received from the status look-up table, we can then take into account, the internal bus capacity (transfer rate), say C bits/sec; then the affine function (Eq.(6)) can be completed with an inequality constraint (this inequality constraint idea was introduced by Georges, Divoux and Rondeau (2005) in relation to the communication link feeding a switch):

$$b(t) \le Ct \quad (7)$$

(7), means that, the arrival of data to the output buffers of a switch cannot be greater than the internal bus capacity through which the data will flow. Eq. (6) can now be completed with the inequality constraint (7) as:

$$b(t)=\min\{Ct, \sigma+\rho t\} \quad (8)$$

We can now write out the amount of data that have arrived in the interval $[s_j, s]$ for all $s_j \geq s$ as:

$$\int_S^{Sj} R_{in}(t)dt \leq \min\{C(s_j - s), \sigma+\rho(s_j - s)\} \quad (9)$$

From Eq. (8), if $Ct < \sigma + \rho t$, then

$b(t) = Ct$ and $t < \dfrac{\sigma}{C-\rho}$ (10)

$$\frac{db(t)}{dt}=C \quad (11)$$

and if $\sigma+\rho t < Ct$, then

$b(t) = \sigma + \rho t$ and $t > \dfrac{\sigma}{C-\rho}$ (12)

$$\frac{db(t)}{dt}=\rho \quad (13)$$

Eqs. (11) and (13) then gives us two possible arrival rates: C, the internal bus capacity and ρ, a long term average rate (both are in bits/sec).

But the maximum burst size has been defined as the maximum length of time that a data traffic flows at the peak rate (Forouzan, 2008, p.762; Alberto and Widjaja, 2004, p.551); we therefore, ignore Eq. (13) which deals with average rate. Eq. (9) can then be written (taking the upper bound of the inequality) as:

$$\int_S^{Sj} R_{in}(t)dt = C(s_j - s) \quad (14)$$

Eq. (4) now becomes:

$$d_j = \frac{1}{C_{out}} \max_{s \leq s_j} \left[C(s_j - s) - C_{out}(s_j - s)\right] \quad (15)$$

To determine the maximum length of time or max $[s_j - s]$ that the incoming traffic flows at the peak rate, we note that, the upper bound of the inequality of (9) implies,

either $\int_S^{Sj} R_{in}(t)dt = C(s_j - s)$ (16)

or $\int_S^{Sj} R_{in}(t)dt = \sigma+\rho(s_j - s)$ (17)

that is, $C(s_j - s) = \sigma + \rho(s_j - s)$ (18)

or $s_j - s = \dfrac{\sigma}{C-\rho}$ (19)

= maximum length of time at which the traffic flows at the peak rate.

We can now re-write Eq. (15) as:

$$dj = \frac{1}{C_{out}}\left[C\left(\frac{\sigma}{C-\rho}\right) - C_{out}\left(\frac{\sigma}{C-\rho}\right)\right]$$

$$= \frac{1}{C_{out}}\left[\frac{(C-C_{out})\sigma}{C-\rho}\right] \quad (20)$$

= maximum delay in seconds suffered by the j^{th} packet in crossing the FIFO queue.

We note here again that σ is the maximum burst size (in bits) of the input traffic stream to the FIFO Queue. But we had earlier stated that ρ is the rate at which a work-conserving system that accepts data at a rate described by the rate function R transmits the data while there is data to be transmitted. (Cruz, 1991) We can explain this concept in this simple way. Consider a work-conserving system which receives data at a rate described by R(t), and issues out the data at a constant rate C_{out}. It is easy to see that C_{out} also represents the average rate of traffic arrivals to the work-conserving system. This idea was amply illustrated by Sven, Ales, and Stanislav (2008) as is shown in Figure 2. And in the words of Costa, Netto and Pereira (2004), the queuing delay experienced by packets in arriving at a switch varies, since the packets that might have arrived in the output queue before any arriving packet, is not fixed; it depends on the patterns of arrivals at any time.

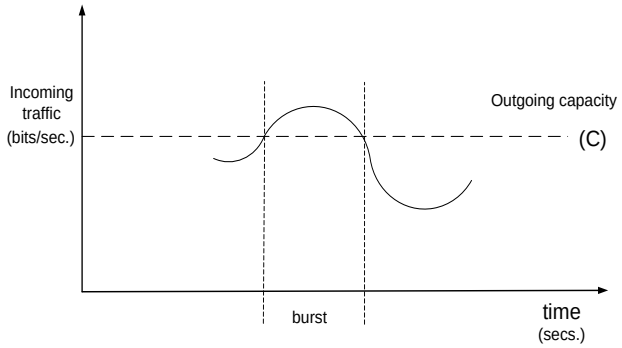

Fig. 2 Illustration of traffic arrivals to and departures from a queuing system with constant output rate, C.
source : [10]

Therefore, taking ρ as C_{out}, Eq. (20) becomes:

$$d_j = \frac{\sigma}{C_{out}} \tag{21}$$

where:
d_j = maximum delay in seconds suffered by the j^{th} packet in crossing the FIFO Queue,
σ = maximum amount of data traffic that can arrive in a burst in bits,
C_{out} = bit rate of the output link(switch port) in bits per second(bps).

Eq. (21) is in agreement with the assertion (with respect to a router) by Sven, Ales and Stanislav (2008), that, since the output queue of a router is emptied at the nominal link capacity, an hypothesis can be made that, the size of a packet burst in bits measured on a router output port divided by the nominal physical link capacity is the upper limit of delay added to the queue build-up by the packet burst. We have, however, shown beyond this hypothesis that Eq. (21) actually characterizes the maximum delay suffered by a packet at the output queue of the output port of a switch (since a router is a switching device).

3. CONCLUSION

The queuing delay which is suffered by a packet that is transiting a packet switch has the most adverse effect on the performance of the packet switch. Being able to estimate the maximum queuing delay which any packet may suffer in a packet switch will make the designs of upper bounded end-to-end delay switched networks possible. In this paper, we have shown in consonance with literature definitions that the maximum queuing delay of a packet switch is the maximum size of traffic that can arrive to the switch in a burst divided by the nominal link capacity of the output port through which the arrived traffic will exit the switch.

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